

Application number 09/606,252
Amendment dated February 2, 2004
Reply to office action mailed July 31, 2003

PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-26 (cancelled)

Claim 27 (currently amended) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate;

implanting a field implant;

implanting a well implant;

implanting an enhancement implant;

forming a gate oxide on the semiconductor substrate;

forming a gate on the gate oxide;

implanting a first pocket implant into the semiconductor substrate from a first side of the gate; and

implanting a second pocket implant into the semiconductor substrate from a second side of the gate,

adjusting a short channel effect of the transistor by diffusing the first pocket implant and the second pocket implant laterally in the semiconductor substrate;

wherein the implanting the field implant, the well implant, and the enhancement implant are done using a single mask, and the first pocket implant and the second pocket implant are in contact at about the center of a channel region.

Claim 28 (cancelled)

Claim 29 (previously presented) The method of claim 27 wherein the first pocket implant and the second pocket implant are implanted at an angle.

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Claim 30 (previously presented) The method of claim 27 wherein the first pocket implant and the second pocket implant are implanted using the gate as a mask.

Claim 31 (currently amended) The method of claim 28 27 wherein the diffusing increases a reverse short channel effect of the transistor.

Claim 32 (cancelled)

Claim 33 (previously presented) The method of claim 27 further comprising forming a source on the first side of the gate and a drain on the second side of the gate, wherein the source and drain are doped at a first polarity and the first pocket implant and the second pocket implant are doped at a second polarity.

Claim 34 (previously presented) The method of claim 33 wherein the first polarity is different than the second polarity.

Claim 35 (currently amended) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate;
forming a gate oxide on the semiconductor substrate;
forming a gate on the gate oxide;
implanting a first pocket implant and a second pocket implant into the semiconductor substrate using the gate as a mask; and
adjusting a short channel effect of the transistor by diffusing the first and second pocket implants laterally causing the first pocket implant to merge with the second pocket implant.

Claim 36 (previously presented) The method of claim 35 wherein the diffusing increases a reverse short channel effect of the transistor.

Claim 37 (previously presented) The method of claim 35 further comprising implanting an enhancement implant in the semiconductor substrate.

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Claim 38 (previously presented) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate having a surface;
forming a gate oxide on the semiconductor substrate surface;
forming a gate on the gate oxide;
implanting a first pocket implant into the semiconductor substrate from a first side of the gate at an angle;
implanting a second pocket implant into the semiconductor substrate from a second side of the gate at an angle; and
adjusting a threshold voltage of the transistor by diffusing the first and second pocket implants laterally.

Claim 39 (cancelled)

Claim 40 (previously presented) The method of claim 38 wherein the first pocket implant and the second pocket implant are implanted using the gate as a mask.

Claim 41 (cancelled)

Claim 42 (previously presented) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate having a surface;
forming a gate oxide on the semiconductor substrate surface;
forming a gate on the gate oxide;
implanting a first pocket implant into the semiconductor substrate from a first side of the gate at an angle;
implanting a second pocket implant into the semiconductor substrate from a second side of the gate at an angle; and
adjusting a short channel effect of the transistor by diffusing the first and second pocket implants laterally.

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Claim 43 (previously presented) The method of claim 42 wherein the diffusing increases a threshold voltage of the transistor.

Claim 44 (previously presented) The method of claim 42 further comprising implanting an enhancement implant in the semiconductor substrate.

Claim 45 (previously presented) The method of claim 35 further comprising:
implanting a field implant;
implanting a well implant; and
implanting an enhancement implant,
wherein the implanting the field implant, the well implant, and the enhancement implant are done using a single mask.

Claim 46 (previously presented) The method of claim 38 further comprising:
implanting a field implant;
implanting a well implant; and
implanting an enhancement implant,
wherein the implanting the field implant, the well implant, and the enhancement implant are done using a single mask.

Claim 47 (previously presented) The method of claim 42 further comprising:
implanting a field implant;
implanting a well implant; and
implanting an enhancement implant,
wherein the implanting the field implant, the well implant, and the enhancement implant are done using a single mask.